AMENDMENT TO CLAIMS

1. (Currently amended) A semiconductor device comprising:

first and second circuit blocks provided on a semiconductor chip and including respective functional elements; and

a timing adjustment circuit block provided between the first and second circuit blocks for adjusting a propagation timing of a transmission signal flowing on a line connecting the first and second circuit blocks to each other.

2. (Original) The semiconductor device of claim 1, further comprising a comparison control circuit for receiving an input signal input to the first circuit block and an output signal output from the second circuit block which has received the transmission signal, comparing the input signal to the output signal, and controlling the timing adjustment circuit block.

3. (Currently amended) [[The]] A semiconductor device comprising: ~~of claim 1,~~

first and second circuit blocks provided on a semiconductor chip and including respective functional elements; and

a timing adjustment circuit block for adjusting a propagation timing of a transmission signal flowing on a line connecting the first and second circuit blocks to each other,

wherein the line comprises a plurality of parallel lines, and

each of the first and second circuit blocks includes a shift register connected to the plurality of lines.

4. (Original) The semiconductor device of claim 2, wherein the comparison control circuit includes a comparison circuit for comparing logical values obtained by performing logical operation on the input signal and the output signal and outputting the comparison result.

5. (Original) The semiconductor device of claim 1, further comprising an input pattern generating circuit for generating and outputting the input signal to the first circuit block.

6. (Currently amended) [[The]] A semiconductor device comprising: ~~of claim 1,~~

first and second circuit blocks provided on a semiconductor chip and including respective functional elements; and

a timing adjustment circuit block for adjusting a propagation timing of a transmission signal flowing on a line connecting the first and second circuit blocks to each other,

wherein the timing adjustment circuit block includes a first holding circuit for holding update information in which the propagation timing of the transmission signal is updated.

7. (Original) The semiconductor device of claim 6, wherein the first holding circuit includes at least one fuse.

8. (Original) The semiconductor device of claim 6, wherein the timing adjustment circuit block includes a second holding circuit for holding update information in which the propagation timing of the transmission signal is updated, and

the second holding circuit performs a parallel-to-serial conversion on the update information and outputs the conversion result.

9. (Original) The semiconductor device of claim 3, wherein the timing adjustment circuit block repeatedly adjusts the propagation timing of the transmission signal until the input signal and the output signal become the same.

10. (Original) The semiconductor device of claim 9, wherein the timing adjustment circuit block includes a circuit for outputting an adjustment termination notification signal for notifying that adjustments of the propagation timings of all the transmission signals flowing on the lines terminate, and

the adjustments of the propagation timings terminate when the input signal and the output signal become the same or when the adjustment termination notification signal is output.

11. (Currently amended) [[The]] A semiconductor device comprising: ~~of claim 2,~~

first and second circuit blocks provided on a semiconductor chip and including respective functional elements;

a timing adjustment circuit block for adjusting a propagation timing of a transmission signal flowing on a line connecting the first and second circuit blocks to each other; and

a comparison control circuit for receiving an input signal input to the first circuit block and an output signal output from the second circuit block which has received the transmission signal, comparing the input signal to the output signal, and controlling the timing adjustment circuit block,

wherein the comparison control circuit includes a control circuit for outputting timing adjustment control signals to the timing adjustment circuit block when the comparison result shows that the input signal and the output signal differ from each other,

the timing adjustment circuit block includes:

a counter circuit for receiving the timing adjustment control signals, and counting and electrically holding the number of the received timing adjustment control signals;

a delay element block which includes at least one delay element and in which a delay amount depending on the number of the timing adjustment control signals is added to the transmission signal; and

a fuse circuit which includes at least one fuse and holds the number of the timing adjustment control signals in correspondence with the number of fuses which are melted down,

wherein an output signal from the counter circuit or an output signal from the fuse circuit is selectively input to the delay element block, and

the fuse is melted down based on the output signal from the counter circuit.

12. (Original) The semiconductor device of claim 11, further comprising a switching circuit which generates and outputs a switching control signal for selecting one of the output signals from the counter circuit and the fuse circuit and which includes a fuse.

13. (Original) The semiconductor device of claim 11, wherein if a result of a verification performed on the propagation timing of the transmission signal is true, the output signal from the counter circuit is switched to the output signal from the fuse circuit.

14. (Original) The semiconductor device of claim 11, wherein the counter circuit has a high output impedance in normal operation, whereas the fuse circuit has a high output impedance in a verification.

15. (Original) The semiconductor device of claim 11, wherein the line comprises a plurality of parallel lines, and

the counter circuit and the fuse circuit share the timing adjustment control signals for respective transmission signals flowing on the plurality of lines.

16. (Original) The semiconductor device of claim 11, wherein the timing adjustment circuit block is also capable of adjusting a propagation timing of a clock signal for determining the propagation timing of the transmission signal.

17. (Original) The semiconductor device of claim 16, wherein the propagation timing of the clock signal is adjusted when the adjustment of the propagation timing of the transmission signal fails.

18. (Original) The semiconductor device of claim 16, wherein the counter circuit is reset every time the propagation timing of the clock signal is adjusted.

19. (Original) The semiconductor device of claim 17, wherein the timing adjustment circuit block includes a determination circuit for receiving the output signal from the counter circuit, determining whether the adjustment of the propagation timing of the transmission signal

has succeeded or not, and, if it is determined that the adjustment of the propagation timing of the transmission signal has succeeded, outputting a termination signal for terminating a timing verification.

20. (Original) The semiconductor device of claim 19, wherein the termination signal is output when the number of signals input to the determination circuit exceeds a given value.

21. (Currently amended) The semiconductor device of claim 1, wherein the timing adjustment circuit block includes:

a determination period [[pulse]] signal generating circuit for generating and outputting a determination period [[pulse]] signal for determining the propagation timing of the transmission signal, based on a clock signal for determining the propagation timing of the transmission signal;

a delay element block which includes at least one delay element and in which a delay is added to the transmission signal; and

a fuse circuit which includes at least one fuse, the fuse being melted down based on the determination period [[pulse]] signal and a transmission signal which has passed through the delay element block.

22. (Original) The semiconductor device of claim 21, wherein the pulse signal is a signal having a signal determination period including at least one of a set-up period and a hold period of the transmission signal with respect to the clock signal.

23. (Original) The semiconductor device of claim 22, wherein the pulse signal allows at least one of the set-up period and the hold period to be selected with a signal from the outside.

24. (Original) The semiconductor device of claim 21, wherein the pulse signal generating circuit generates the pulse signal by performing logical operation on the clock signal and the transmission signal.

25. (Original) The semiconductor device of claim 24, wherein the pulse signal is output to the outside.

26. (Original) The semiconductor device of claim 21, wherein the propagation timing of the transmission signal is repeatedly adjusted until the adjustment is completed.

27. (Currently amended) [[The]] A semiconductor device ~~of claim 2, further~~ comprising:

first and second circuit blocks provided on a semiconductor chip and including respective functional elements;

a timing adjustment circuit block for adjusting a propagation timing of a transmission signal flowing on a line connecting the first and second circuit blocks to each other;

a comparison control circuit for receiving an input signal input to the first circuit block and an output signal output from the second circuit block which has received the transmission signal, comparing the input signal to the output signal, and controlling the timing adjustment circuit block; and

an input pattern generating circuit for generating and outputting the input signal to the first circuit block,

wherein the input pattern generating circuit is activated when the comparison result from the comparison control circuit shows that the input signal and the output signal differ from each other.

28. (Original) The semiconductor device of claim 6, wherein the first holding circuit is a nonvolatile memory circuit.

29. (Original) The semiconductor device of claim 28, wherein the timing adjustment circuit block includes a second holding circuit for holding update information in which the propagation timing of the transmission signal is updated, and

the update information is written into the nonvolatile memory circuit from the second holding circuit after a verification of the propagation timing terminates.

30. (Original) The semiconductor device of claim 28, further comprising an internal power-supply circuit for supplying a power-supply voltage to the nonvolatile memory circuit.

31. (Original) The semiconductor device of claim 28, wherein a power-supply voltage is supplied to the nonvolatile memory circuit from the outside.

32. (Currently amended) [[The]] A semiconductor device comprising: ~~of claim 2,~~

first and second circuit blocks provided on a semiconductor chip and including respective functional elements;

a timing adjustment circuit block for adjusting a propagation timing of a transmission signal flowing on a line connecting the first and second circuit blocks to each other; and

a comparison control circuit for receiving an input signal input to the first circuit block and an output signal output from the second circuit block which has received the transmission signal, comparing the input signal to the output signal, and controlling the timing adjustment circuit block,

wherein the comparison control circuit includes a control circuit for outputting timing adjustment control signals to the timing adjustment circuit block when the comparison result shows that the input signal and the output signal differ from each other,

the timing adjustment circuit block includes:

a counter circuit for receiving the timing adjustment control signals, and counting and electrically holding the number of the received timing adjustment control signals;

a delay element block which includes at least one delay element and in which a delay amount depending on the number of the timing adjustment control signals is added to the transmission signal; and

a nonvolatile memory circuit,

wherein an output signal from the counter circuit or an output signal from the nonvolatile memory circuit is selectively input to the delay element block, and

the number of the timing adjustment control signals is written into the nonvolatile memory circuit based on the output signal from the counter circuit.

33. (Original) The semiconductor device of claim 32, wherein every time the output value of the counter circuit changes, the output value is written into the nonvolatile memory circuit.

34. (Original) The semiconductor device of claim 33, wherein the output value is written into the nonvolatile memory circuit only during a verification of the propagation timing of the transmission signal.

35. (Original) The semiconductor device of claim 32, wherein the nonvolatile memory circuit is connected to the delay element block after a verification of the propagation timing of the transmission signal.

36. (Original) The semiconductor device of claim 1, wherein one of the first and second circuit blocks is a memory circuit block.

37. (Currently amended) [[The]] A semiconductor device ~~of claim 36, further~~ comprising:

first and second circuit blocks provided on a semiconductor chip and including respective functional elements, one of the first and second circuit blocks being a memory circuit block;

a timing adjustment circuit block for adjusting a propagation timing of a transmission signal flowing on a line connecting the first and second circuit blocks to each other; and

an output timing changing circuit for changing the timing of outputting an output signal from the memory circuit block in synchronization with a change of the propagation timing of a clock signal for determining the propagation timing of the transmission signal.

38. (Original) The semiconductor device of claim 37, wherein the output timing changing circuit is provided inside the memory circuit block.